10-Bit Bidirectional Low-Voltage Translator

GTL2010PW

アーカイブス

このページには、製造中止（生産終了）となった製品の情報が記載されています。本ページに記載されている仕様および情報は、過去の参考情報です。

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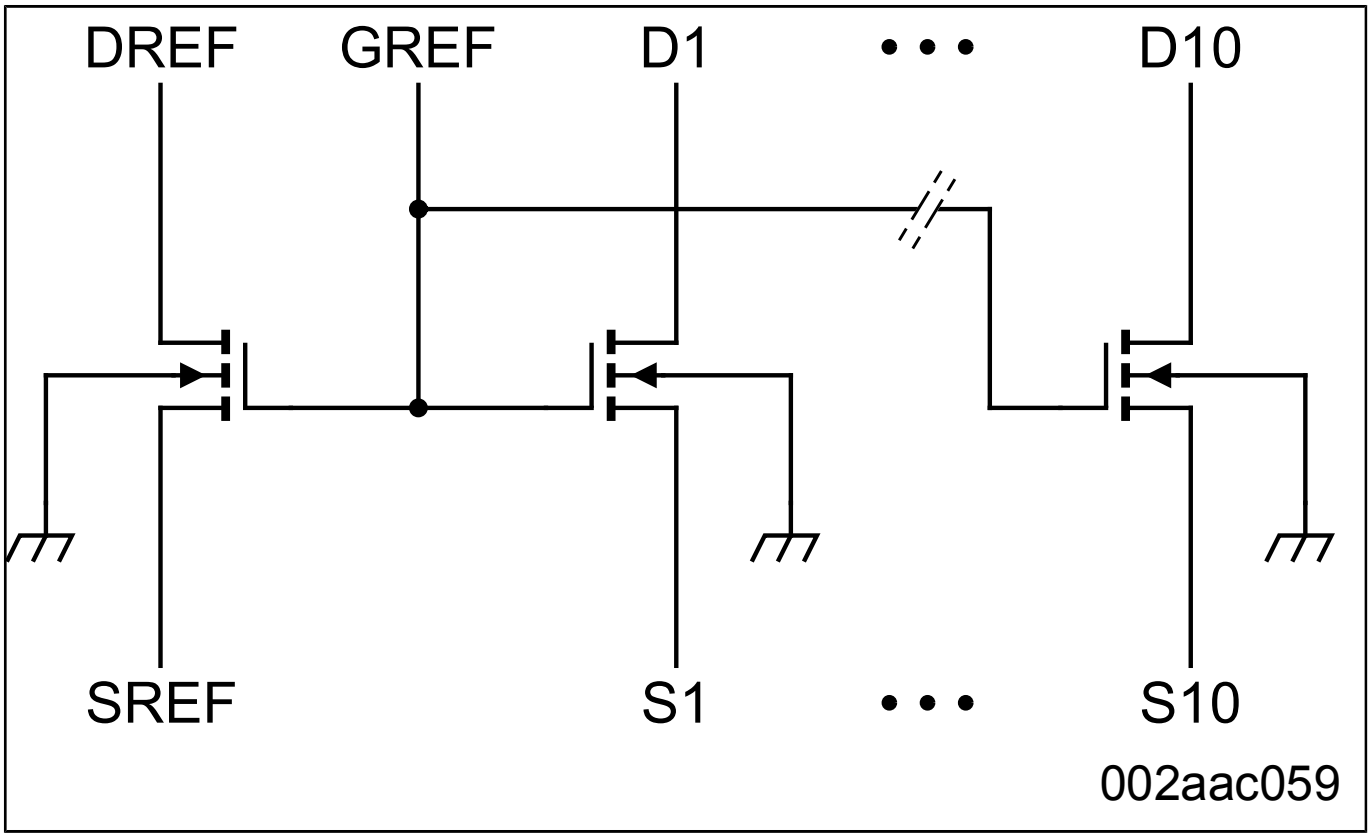
The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2010 provides 10 NMOS pass transistors (Sn and Dn) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bidirectional voltage translations between 1.0 V and 5.0 V without use of a direction pin.

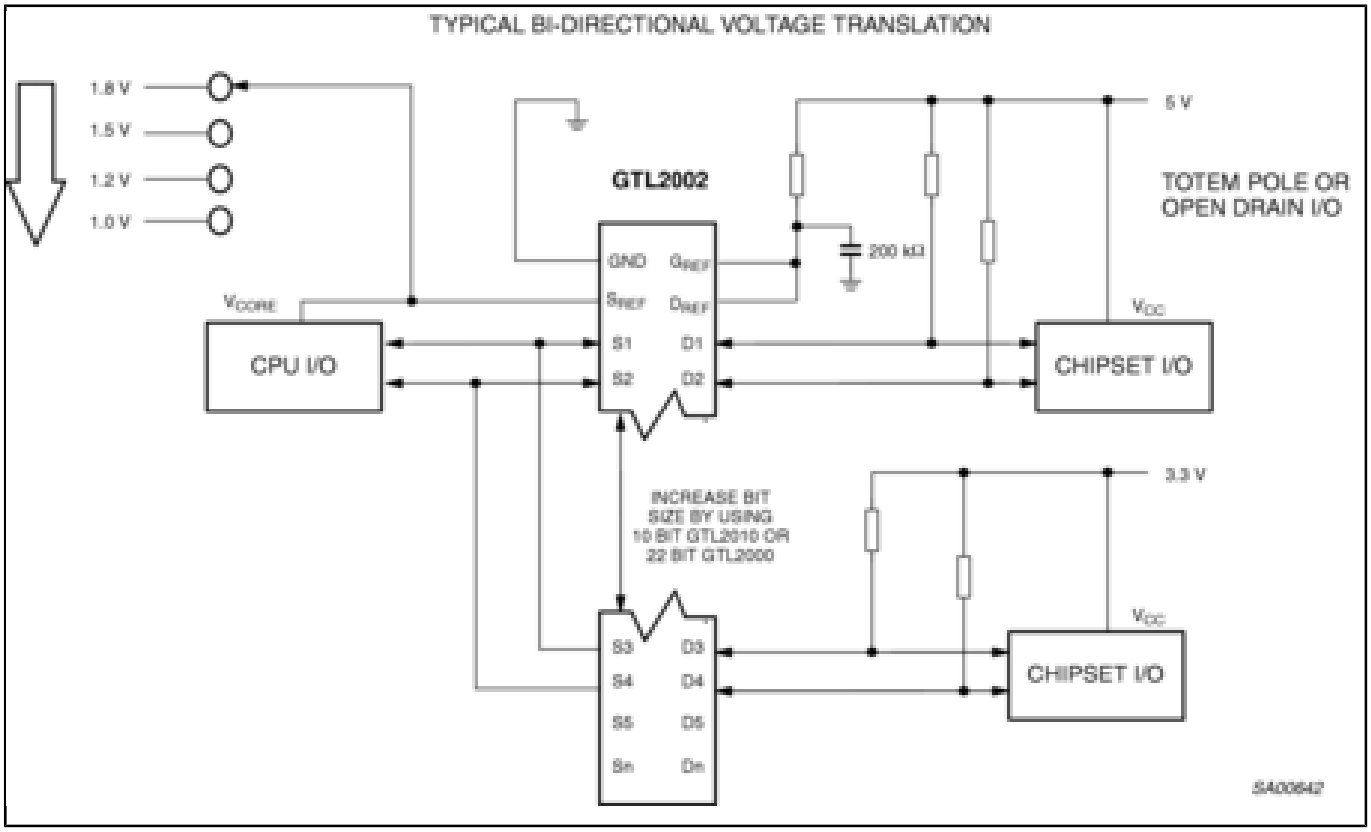
When the Sn or Dn port is LOW, the clamp is in the ON-state and a low resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH the voltage on the Sn port is limited to the voltage set by the reference transistor (SREF). When the Sn port is HIGH, the Dn port is pulled to VCC by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other ten matched Sn/Dn transistors, allowing for easier board layout. The translator's transistors provide excellent ESD protection to lower voltage devices and at the same time protect less ESD-resistant devices.

GTL2010 Block Diagram



GTL2000DGG, GTL2000DL, GTL2010BS, GTL2010PW Block Diagram



View additional information for 10-Bit Bidirectional Low-Voltage Translator.

Note: The information on this document is subject to change without notice.