



13-Bit GTL-/GTL/GTL+ to LVTTTL Translator

GTL2006PW

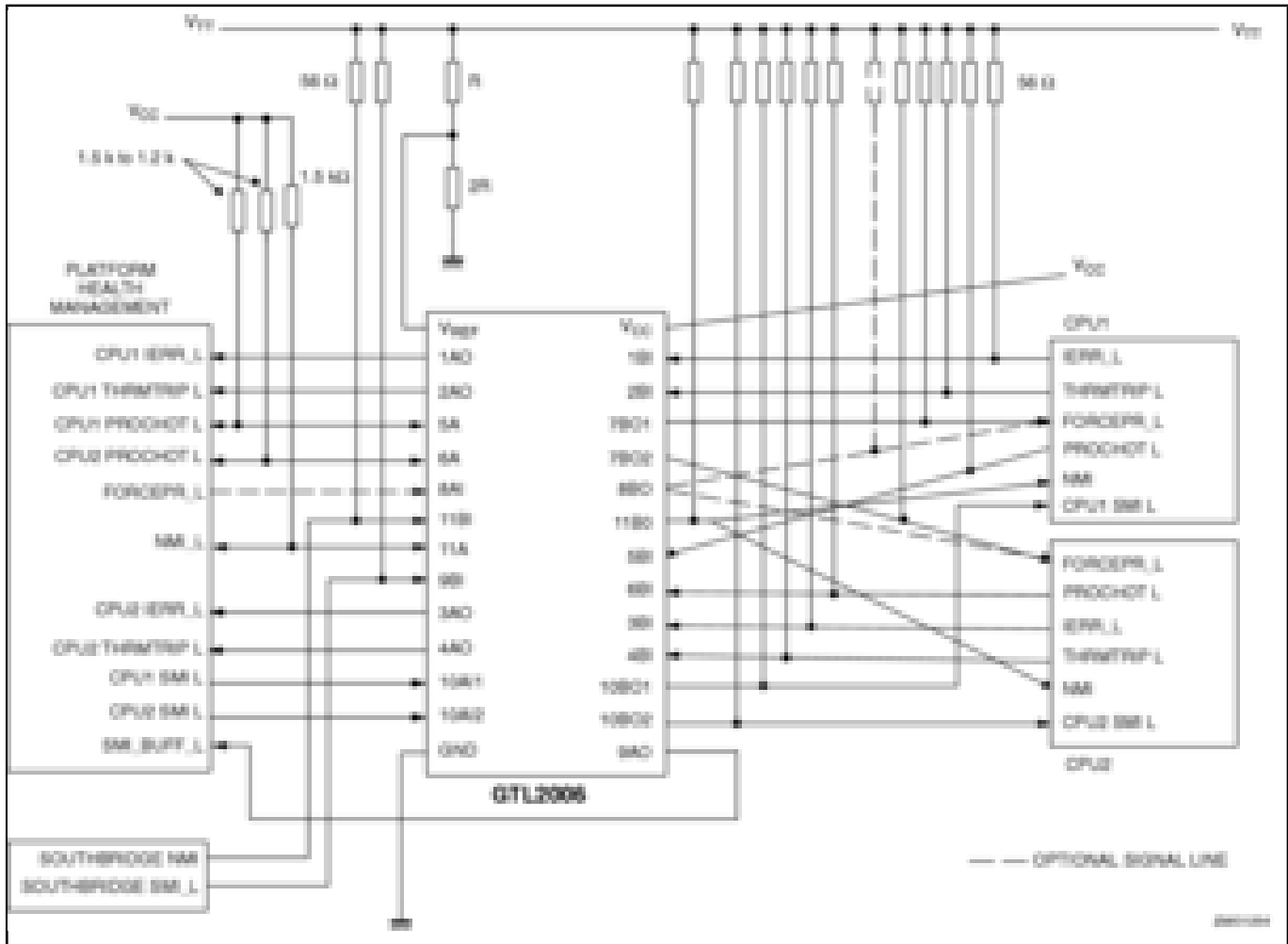
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Last Updated: Jun 14, 2023

The GTL2006 is a 13-bit translator to interface between the 3.3 V LVTTTL chip set I/O and the Xeon™ processor GTL-/GTL/GTL+ I/O. The GTL2006 is designed for platform health management in dual processor applications.

Block diagram: GTL2006PW Block Diagram



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