



8-Bit Bidirectional Low-Voltage Translator

GTL2003

Archived

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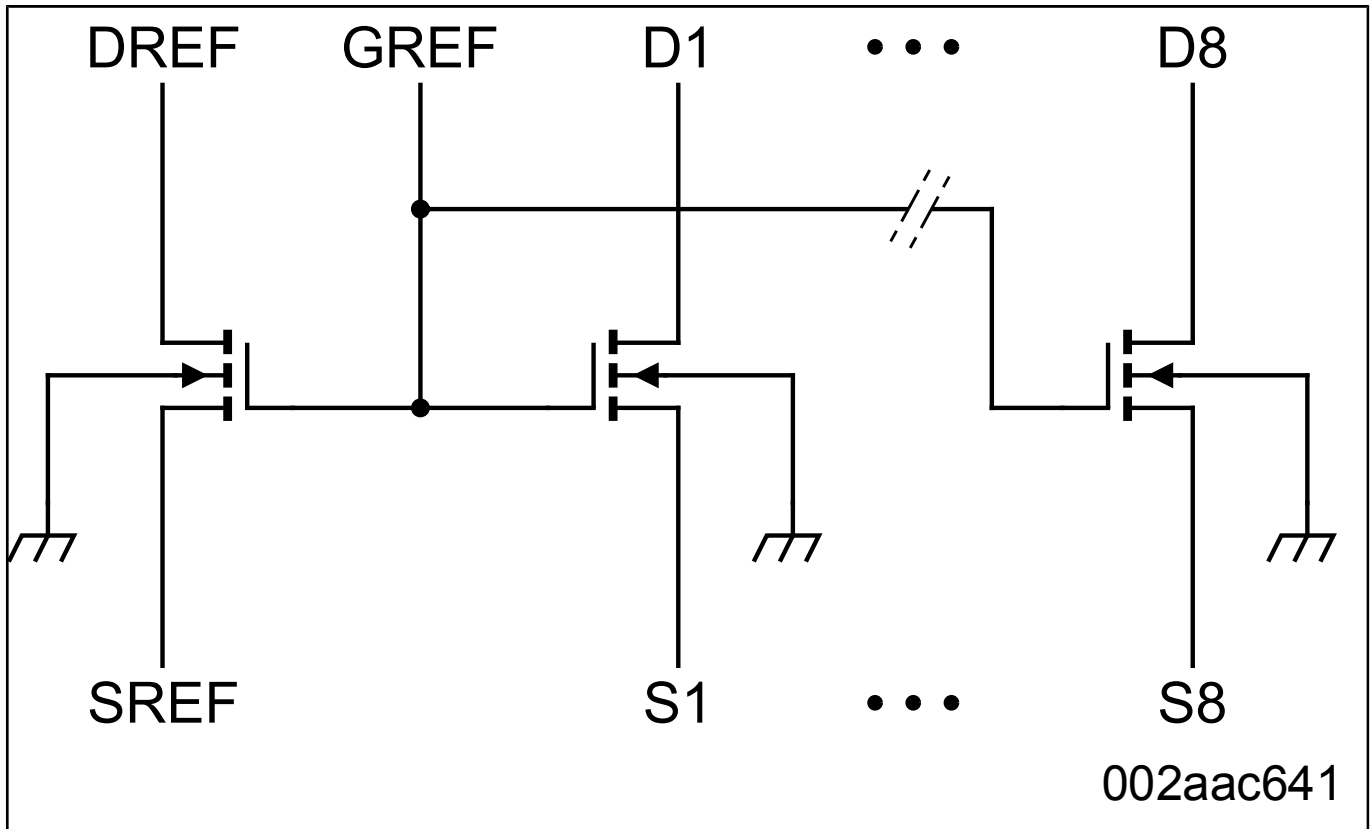
Last Updated: Mar 4, 2025

The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2003 provides eight NMOS pass transistors (S_n and D_n) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bidirectional voltage translations between 0.8 V and 5.0 V without use of a direction pin. Voltage translation below 0.8 V can be achieved when properly biased. For more information, refer to application note AN11127.

When the S_n or D_n port is LOW, the clamp is in the ON-state and a low resistance connection exists between the S_n and D_n ports. Assuming the higher voltage is on the D_n port, when the D_n port is HIGH, the voltage on the S_n port is limited to the voltage set by the reference transistor (SREF). When the S_n port is HIGH, the D_n port is pulled to VDD1 by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other eight matched S_n/D_n transistors, allowing for easier board layout. The translator's transistors provide excellent ESD protection to lower voltage devices and at the same time protect less ESD-resistant devices.

GTL2003 Block Diagram Block Diagram



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