



22-Bit Bidirectional Low-Voltage Translator

GTL2000DGG

アーカイブス

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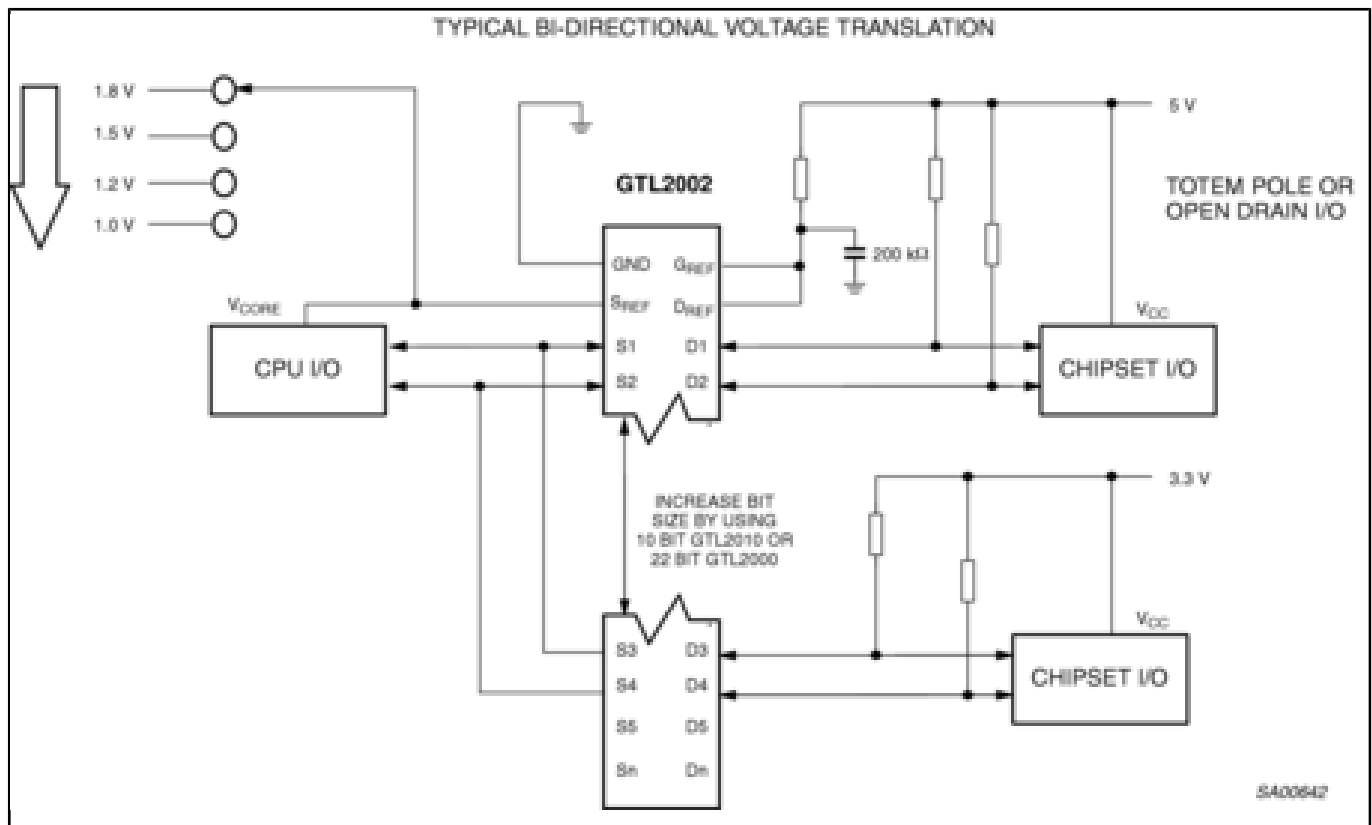
The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2000 provides 22 NMOS pass transistors (S_n and D_n) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bi-directional voltage translations between 1.0 V and 5.0 V without use of a direction pin.

When the S_n or D_n port is low the clamp is in the ON-state and a low resistance connection exists between the S_n and D_n ports. Assuming the higher voltage is on the D_n port, when the D_n port is high, the voltage on the S_n port is limited to the voltage set by the reference transistor (SREF). When the S_n port is high, the D_n port is pulled to VCC by the pull up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other twenty-two matched S_n/D_n transistors, allowing for easier board layout. The translator transistors provides excellent ESD protection to lower voltage devices and at the same time protect less ESD resistant devices.

The open drain construction with no direction pin is ideal for bi-directional low voltage (e.g., 1.0 V, 1.2 V, 1.5 V, or 1.8 V) processor I²C port translation to the normal 3.3 V and/or 5.0 V I²C bus signal levels or GTL/GTL+ translation to LVTTTL/TTL signal levels

GTL2000 Block Diagram Block Diagram



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